

## OP07x Precision Operational Amplifiers

Check for Samples: [OP07C](#), [OP07D](#)

### FEATURES

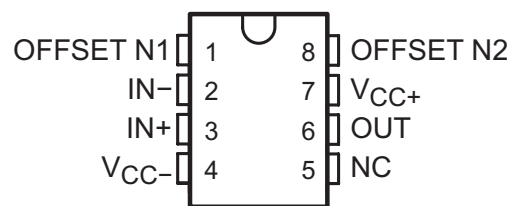
- **Low Noise**
- **No External Components Required**
- **Replace Chopper Amplifiers at a Lower Cost**
- **Wide Input-Voltage Range: 0 to  $\pm 14$  V Typ**
- **Wide Supply-Voltage Range:  $\pm 3$  V to  $\pm 18$  V**

### DESCRIPTION

These devices offer low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range. The OP07 devices are unsurpassed for low-noise, high-accuracy amplification of very-low-level signals.

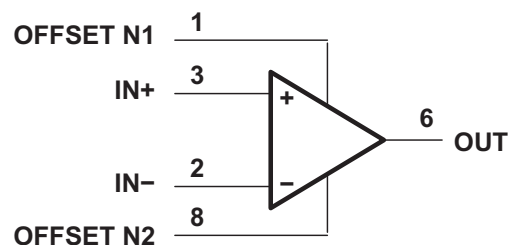
These devices are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**D OR P PACKAGE  
(TOP VIEW)**



NC – No internal connection

**Symbol**



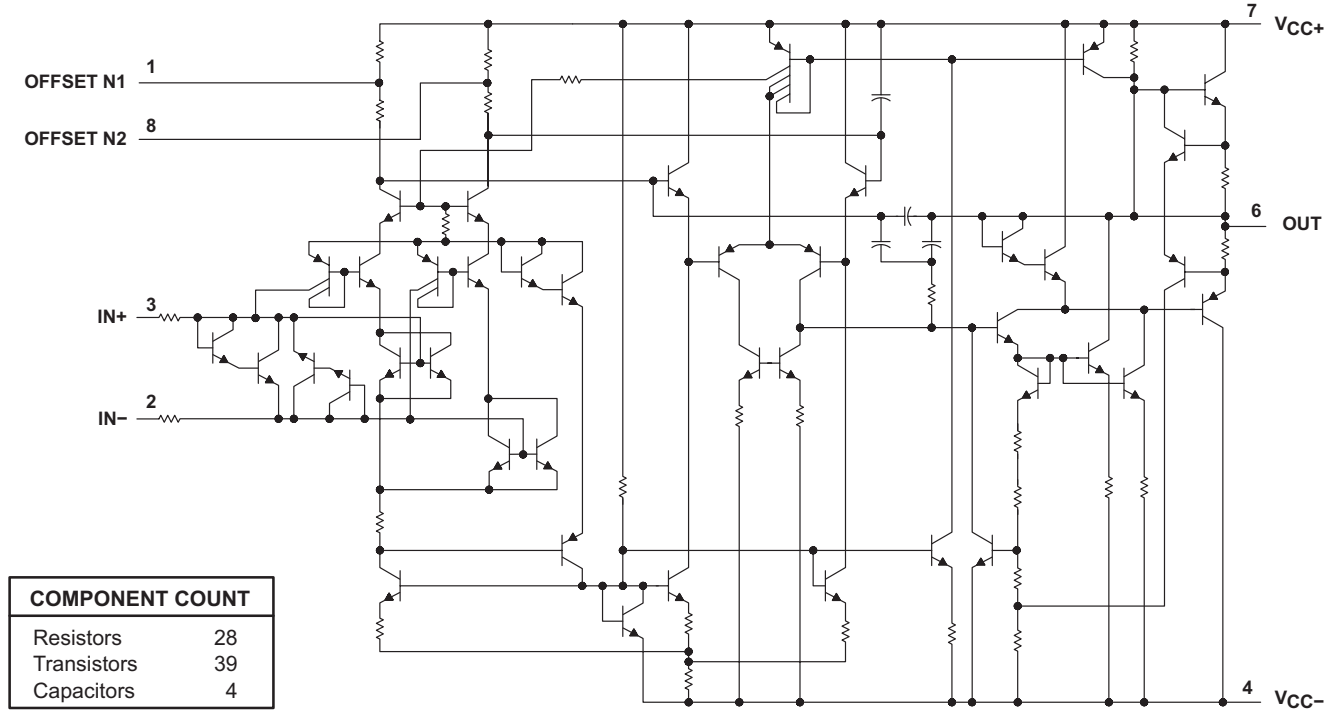
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# OP07C, OP07D

SLOS099F – OCTOBER 1979 – REVISED JANUARY 2014

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## Schematic



Current values shown are nominal.

## Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                                                   |           | MIN       | MAX | UNIT |
|-----------------|-------------------------------------------------------------------|-----------|-----------|-----|------|
| $V_{CC+}^{(2)}$ | Supply voltage                                                    |           |           | 22  | V    |
| $V_{CC-}^{(2)}$ |                                                                   |           |           | –22 |      |
|                 | Differential input voltage <sup>(3)</sup>                         |           |           | ±30 | V    |
| $V_I$           | Input voltage range (either input) <sup>(4)</sup>                 |           |           | ±22 | V    |
|                 | Duration of output short circuit <sup>(5)</sup>                   |           | Unlimited |     |      |
| $\theta_{JA}$   | Package thermal impedance, junction to free air <sup>(6)(7)</sup> | D package |           | 97  | °C/W |
|                 |                                                                   | P package |           | 85  |      |
| $T_J$           | Operating virtual-junction temperature                            |           |           | 150 | °C   |
|                 | Lead temperature 1,6 mm (1/16 in) from case for 10 s              |           |           | 260 | °C   |
| $T_{stg}$       | Storage temperature range                                         |           | –65       | 150 | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, unless otherwise noted, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
- (3) Differential voltages are at  $IN+$  with respect to  $IN-$ .
- (4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
- (5) The output may be shorted to ground or to either power supply.
- (6) Maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_{J(max)} - T_A)/\theta_{JA}$ . Selecting the maximum of 150°C can affect reliability.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|             |                                |                        | MIN | MAX | UNIT |
|-------------|--------------------------------|------------------------|-----|-----|------|
| $V_{CC\pm}$ | Supply voltage                 |                        | ±3  | ±18 | V    |
| $V_{IC}$    | Common-mode input voltage      | $V_{CC\pm} = \pm 15$ V | –13 | 13  | V    |
| $T_A$       | Operating free-air temperature |                        | 0   | 70  | °C   |

# OP07C, OP07D

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## Electrical Characteristics

at specified free-air temperature,  $V_{CC\pm} = \pm 15\text{ V}$  (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                                                              | TEST CONDITIONS                                                                                  | $T_A$ <sup>(2)</sup> | OP07C      |            |     | OP07D      |            |          | UNIT                         |
|------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------|----------------------|------------|------------|-----|------------|------------|----------|------------------------------|
|                                                                        |                                                                                                  |                      | MIN        | TYP        | MAX | MIN        | TYP        | MAX      |                              |
| $V_{IO}$ Input offset voltage                                          | $V_O = 0\text{ V}$ $R_S = 50\Omega$                                                              | 25°C                 |            | 60         |     |            |            | 150      | $\mu\text{V}$                |
|                                                                        |                                                                                                  | 0°C to 70°C          |            | 85         |     |            |            | 250      |                              |
| $\alpha_{VIO}$ Temperature coefficient of input offset voltage         | $V_O = 0\text{ V}$ $R_S = 50\Omega$                                                              | 0°C to 70°C          |            | 0.5        |     |            |            | 2.5      | $\mu\text{V}/^\circ\text{C}$ |
| Long-term drift of input offset voltage                                | See <sup>(3)</sup>                                                                               |                      |            | 0.4        |     |            |            |          | $\mu\text{V}/\text{mo}$      |
| Offset adjustment range                                                | $R_S = 20\text{ k}\Omega$ , See Figure 1                                                         | 25°C                 |            | $\pm 4$    |     |            |            |          | mV                           |
| $I_{IO}$ Input offset current                                          |                                                                                                  | 25°C                 |            | 0.8        |     |            |            | 6        | nA                           |
|                                                                        |                                                                                                  | 0°C to 70°C          |            | 1.6        |     |            |            | 8        |                              |
| $\alpha_{IIO}$ Temperature coefficient of input offset current         |                                                                                                  | 0°C to 70°C          |            | 12         |     |            |            | 50       | $\text{pA}/^\circ\text{C}$   |
| $I_{IB}$ Input bias current                                            |                                                                                                  | 25°C                 |            | $\pm 1.8$  |     |            |            | $\pm 12$ | nA                           |
|                                                                        |                                                                                                  | 0°C to 70°C          |            | $\pm 2.2$  |     |            |            | $\pm 14$ |                              |
| $\alpha_{IIB}$ Temperature coefficient of input bias current           |                                                                                                  | 0°C to 70°C          |            | 18         |     |            |            | 50       | $\text{pA}/^\circ\text{C}$   |
|                                                                        |                                                                                                  |                      |            |            |     |            |            |          |                              |
| $V_{ICR}$ Common-mode input voltage range                              |                                                                                                  | 25°C                 | $\pm 13$   | $\pm 14$   |     | $\pm 13$   | $\pm 14$   |          | V                            |
|                                                                        |                                                                                                  | 0°C to 70°C          | $\pm 13$   | $\pm 13.5$ |     | $\pm 13$   | $\pm 13.5$ |          |                              |
| $V_{OM}$ Peak output voltage                                           | $R_L \geq 10\text{ k}\Omega$                                                                     | 25°C                 | $\pm 12$   | $\pm 13$   |     | $\pm 12$   | $\pm 13$   |          | V                            |
|                                                                        | $R_L \geq 2\text{ k}\Omega$                                                                      |                      | $\pm 11.5$ | $\pm 12.8$ |     | $\pm 11.5$ | $\pm 12.8$ |          |                              |
|                                                                        | $R_L \geq 1\text{ k}\Omega$                                                                      |                      |            | $\pm 12$   |     |            | $\pm 12$   |          |                              |
|                                                                        | $R_L \geq 2\text{ k}\Omega$                                                                      | 0°C to 70°C          | $\pm 11$   | $\pm 12.6$ |     | $\pm 11$   | $\pm 12.6$ |          |                              |
| $A_{VD}$ Large-signal differential voltage amplification               | $V_{CC} = 15\text{ V}$ , $V_O = 1.4\text{ V}$ to $11.4\text{ V}$ , $R_L \geq 500\text{ k}\Omega$ | 25°C                 | 100        | 400        |     |            | 400        |          | V/mV                         |
|                                                                        | $V_O = \pm 10$ , $R_L = 2\text{ k}\Omega$                                                        | 25°C                 | 120        | 400        |     | 120        | 400        |          |                              |
|                                                                        |                                                                                                  | 0°C to 70°C          | 100        | 400        |     | 100        | 400        |          |                              |
| $B_1$ Unity-gain bandwidth                                             |                                                                                                  | 25°C                 | 0.4        | 0.6        |     | 0.4        | 0.6        |          | MHz                          |
| $r_i$ Input resistance                                                 |                                                                                                  | 25°C                 | 8          | 33         |     | 7          | 31         |          | M $\Omega$                   |
| CMRR Common-mode rejection ratio                                       | $V_{IC} = \pm 13\text{ V}$ , $R_S = 50\Omega$                                                    | 25°C                 | 100        | 120        |     | 94         | 110        |          | dB                           |
|                                                                        |                                                                                                  | 0°C to 70°C          | 97         | 120        |     | 94         | 106        |          |                              |
| $k_{SVS}$ Supply-voltage sensitivity ( $\Delta V_{IO}/\Delta V_{CC}$ ) | $V_{CC\pm} = \pm 3\text{ V}$ to $\pm 18\text{ V}$ , $R_S = 50\Omega$                             | 25°C                 |            | 7          | 32  |            | 7          | 32       | $\mu\text{V}/\text{V}$       |
|                                                                        |                                                                                                  | 0°C to 70°C          |            | 10         | 51  |            | 10         | 51       |                              |
| $P_D$ Power dissipation                                                | $V_O = 0$ , No load                                                                              | 25°C                 |            | 80         | 150 |            | 80         | 150      | mW                           |
|                                                                        | $V_{CC\pm} = \pm 3\text{ V}$ , $V_O = 0$ , No load                                               |                      |            | 4          | 8   |            | 4          | 8        |                              |

- (1) Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first 30 days of operation.
- (2) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

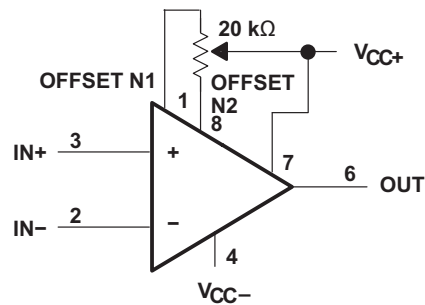
## Operating Characteristics

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

| PARAMETER                                               | TEST CONDITIONS <sup>(1)</sup>      | OP07C | OP07D | UNIT                         |
|---------------------------------------------------------|-------------------------------------|-------|-------|------------------------------|
|                                                         |                                     | TYP   | TYP   |                              |
| $V_n$ Input offset voltage                              | $f = 10\text{ Hz}$                  | 10.5  | 10.5  | $\text{nV}/\sqrt{\text{Hz}}$ |
|                                                         | $f = 100\text{ Hz}$                 | 10.2  | 10.3  |                              |
|                                                         | $f = 1\text{ kHz}$                  | 9.8   | 9.8   |                              |
| $V_{N(PP)}$ Peak-to-peak equivalent input noise voltage | $f = 0.1\text{ Hz to }10\text{ Hz}$ | 0.38  | 0.38  | $\mu\text{V}$                |
| $I_n$ Equivalent input noise current                    | $f = 10\text{ Hz}$                  | 0.35  | 0.35  | $\text{nV}/\sqrt{\text{Hz}}$ |
|                                                         | $f = 100\text{ Hz}$                 | 0.15  | 0.15  |                              |
|                                                         | $f = 1\text{ kHz}$                  | 0.13  | 0.13  |                              |
| $I_{N(PP)}$ Peak-to-peak equivalent input noise current | $f = 0.1\text{ Hz to }10\text{ Hz}$ | 15    | 15    | $\text{pA}$                  |
| SR Slew rate                                            | $R_L \geq 2\text{ k}\Omega$         | 0.3   | 0.3   | $\text{V}/\mu\text{s}$       |

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise noted.

## APPLICATION INFORMATION



**Figure 1. Input Offset-Voltage Null Circuit**

## REVISION HISTORY

| Changes from Revision E (May 2004) to Revision F                                | Page              |
|---------------------------------------------------------------------------------|-------------------|
| • Updated document to new TI data sheet format - no specification changes. .... | <a href="#">1</a> |
| • Deleted Ordering Information table. ....                                      | <a href="#">1</a> |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| OP-07DPSR        | ACTIVE        | SO           | PS                 | 8    | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | OP-07D                  | <a href="#">Samples</a> |
| OP-07DPSRG4      | ACTIVE        | SO           | PS                 | 8    | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | OP-07D                  | <a href="#">Samples</a> |
| OP07CD           | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | OP07C                   | <a href="#">Samples</a> |
| OP07CDE4         | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | OP07C                   | <a href="#">Samples</a> |
| OP07CDG4         | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | OP07C                   | <a href="#">Samples</a> |
| OP07CDR          | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU   CU SN       | Level-1-260C-UNLIM   | 0 to 70      | OP07C                   | <a href="#">Samples</a> |
| OP07CDRE4        | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | OP07C                   | <a href="#">Samples</a> |
| OP07CDRG4        | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | OP07C                   | <a href="#">Samples</a> |
| OP07CP           | ACTIVE        | PDIP         | P                  | 8    | 50             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | OP07CP                  | <a href="#">Samples</a> |
| OP07CPE4         | ACTIVE        | PDIP         | P                  | 8    | 50             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | OP07CP                  | <a href="#">Samples</a> |
| OP07DD           | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | OP07D                   | <a href="#">Samples</a> |
| OP07DDG4         | ACTIVE        | SOIC         | D                  | 8    | 75             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | OP07D                   | <a href="#">Samples</a> |
| OP07DDR          | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | OP07D                   | <a href="#">Samples</a> |
| OP07DDRE4        | ACTIVE        | SOIC         | D                  | 8    | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | OP07D                   | <a href="#">Samples</a> |
| OP07DP           | ACTIVE        | PDIP         | P                  | 8    | 50             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | OP07DP                  | <a href="#">Samples</a> |
| OP07DPE4         | ACTIVE        | PDIP         | P                  | 8    | 50             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | OP07DP                  | <a href="#">Samples</a> |

<sup>(1)</sup> The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

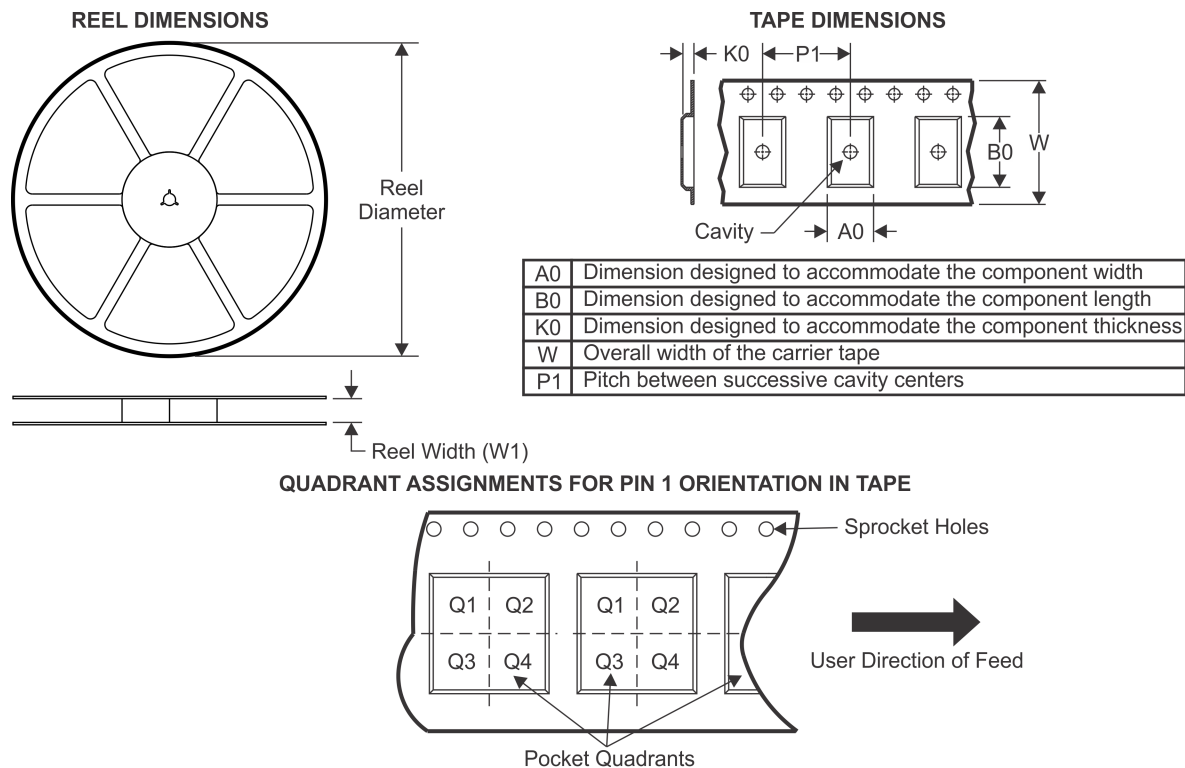
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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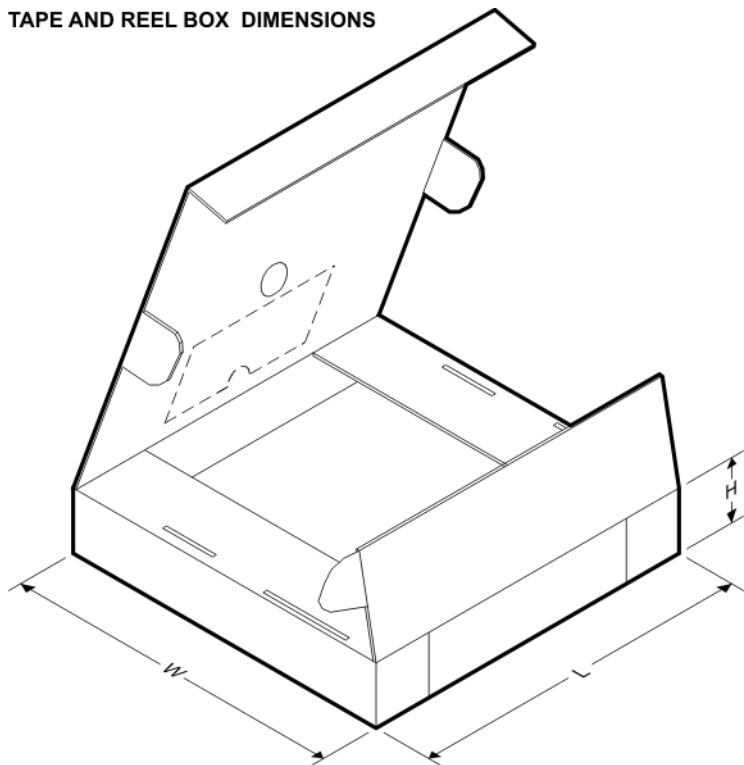


**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| OP-07DPSR | SO           | PS              | 8    | 2000 | 330.0              | 16.4               | 8.2     | 6.6     | 2.5     | 12.0    | 16.0   | Q1            |
| OP07CDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OP07CDRG4 | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| OP07DDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

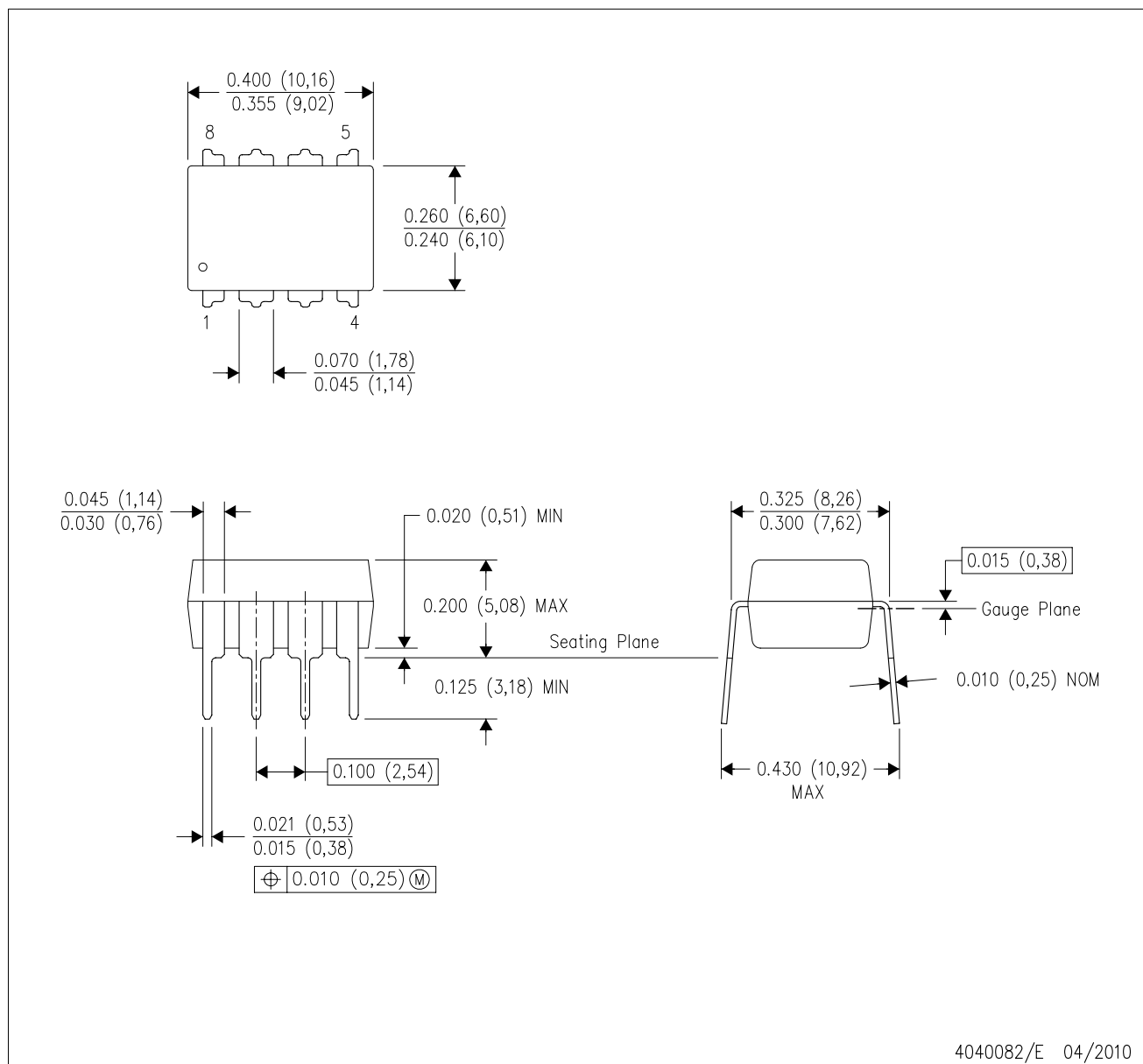


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| OP-07DPSR | SO           | PS              | 8    | 2000 | 367.0       | 367.0      | 38.0        |
| OP07CDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| OP07CDRG4 | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |
| OP07DDR   | SOIC         | D               | 8    | 2500 | 340.5       | 338.1      | 20.6        |

P (R-PDIP-T8)

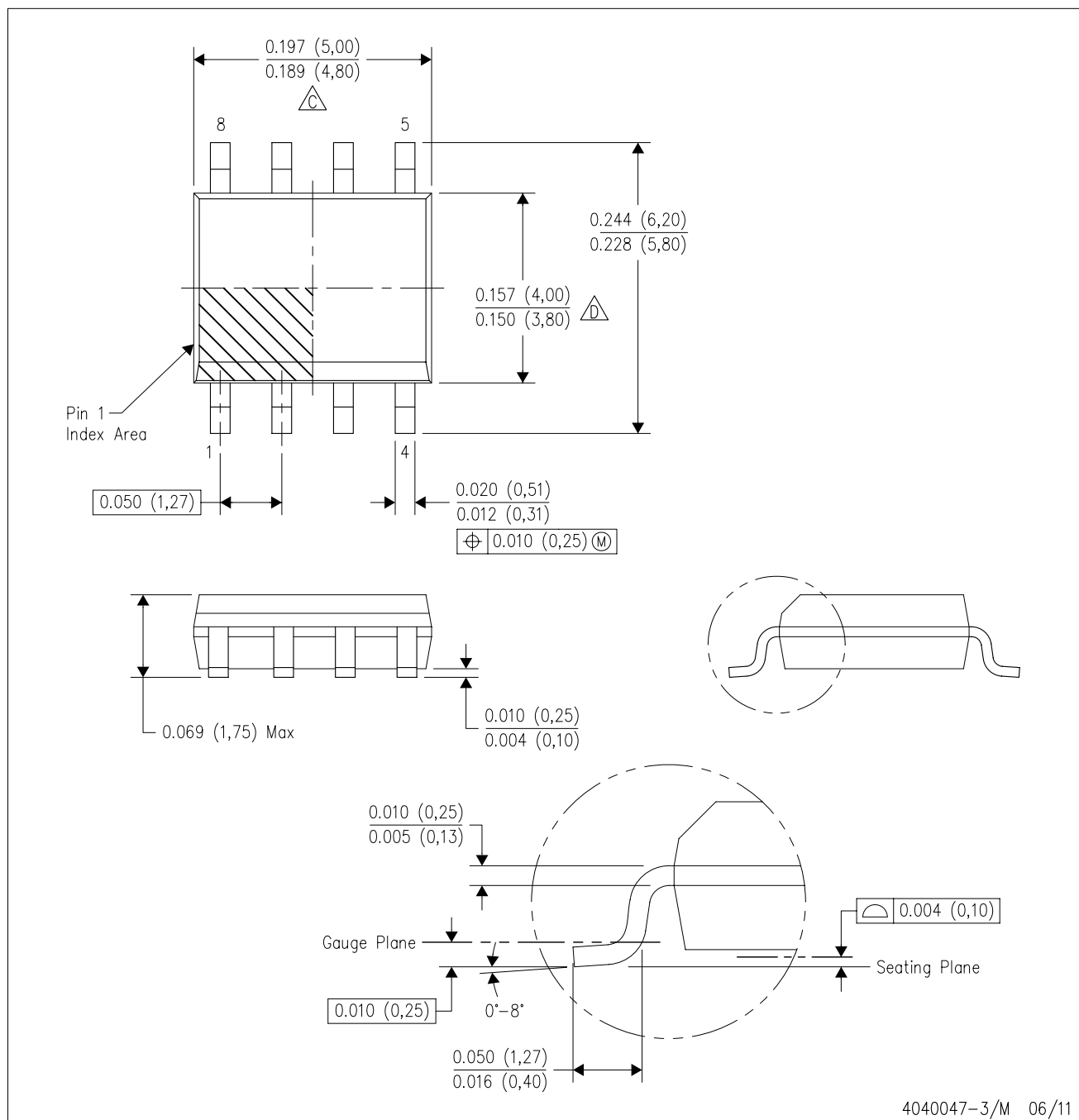
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

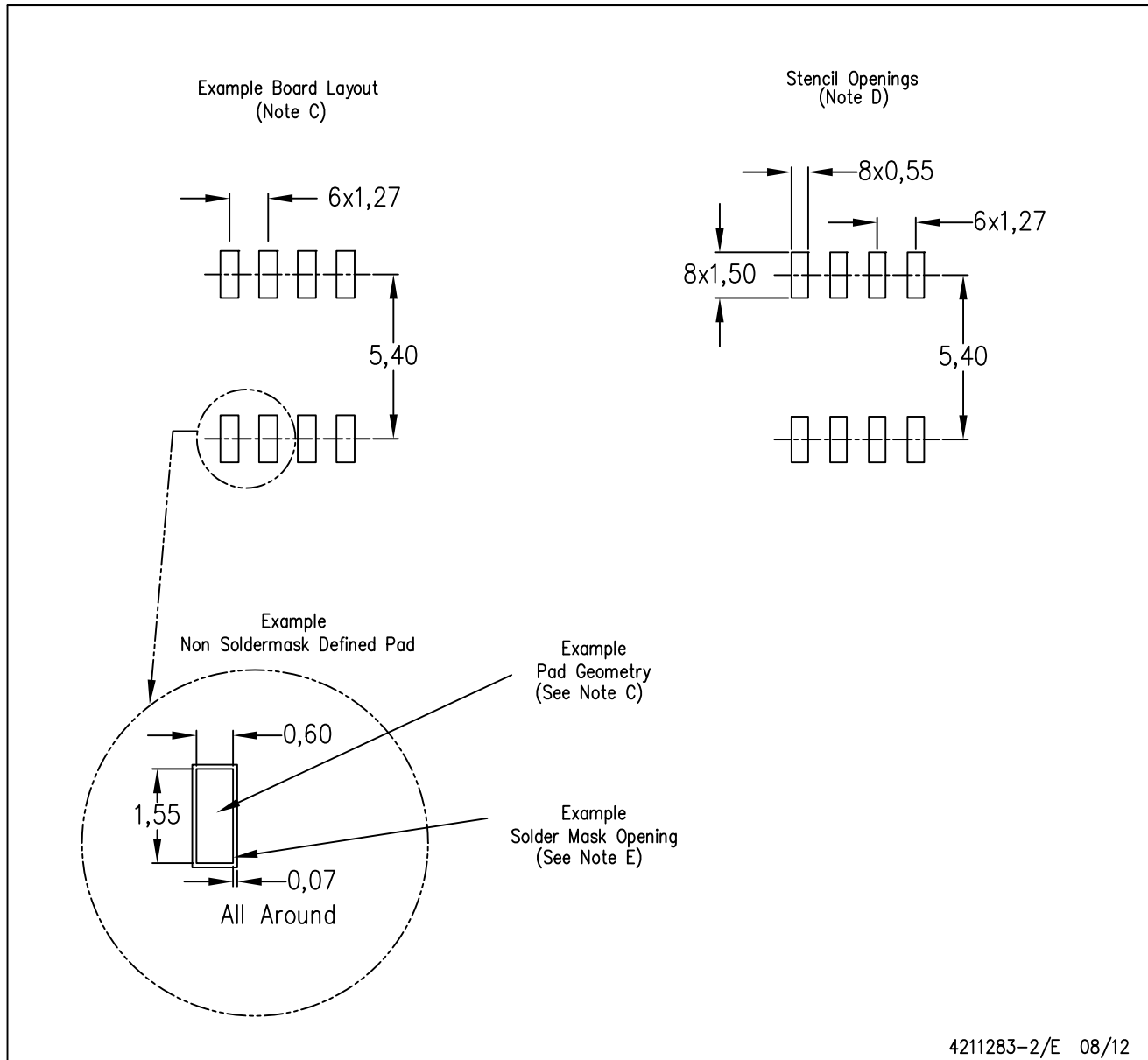
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

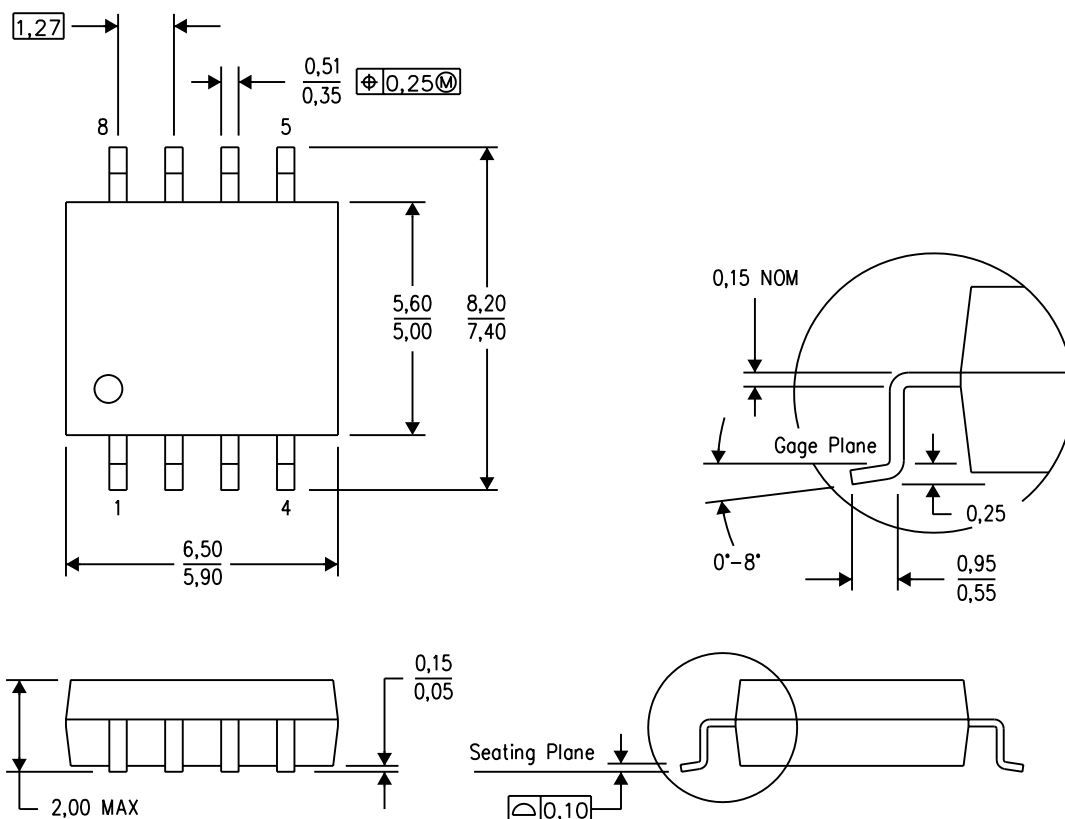


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4040063/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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|                               |                                                                                          |
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