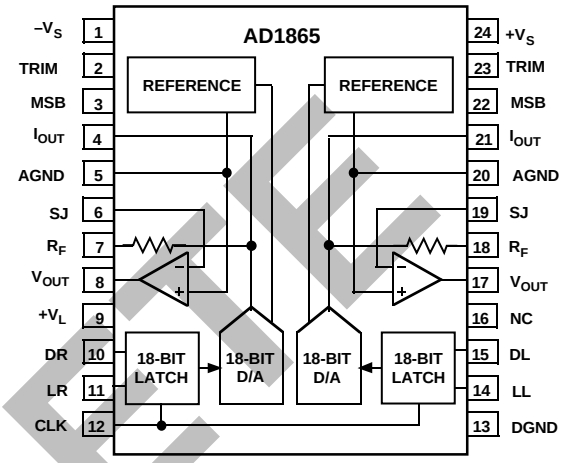
Complete Dual 18-Bit 16 × F_S Audio DAC

AD1865

FEATURES
Dual Serial Input, Voltage Output DACs
No External Components Required
110 dB SNR
0.003% THD+N
Operates at 16 × Oversampling per Channel
±5 Volt Operation
Cophased Outputs
116 dB Channel Separation
Pin Compatible with AD1864
DIP or SOIC Packaging

APPLICATIONS
Multichannel Audio Applications
Compact Disc Players
Multivoice Keyboard Instruments
DAT Players and Recorders
Digital Mixing Consoles
Multimedia Workstations

FUNCTIONAL BLOCK DIAGRAM
(DIP Package)



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD1865 is a complete, dual 18-bit DAC offering excellent THD+N and SNR while requiring no external components. Two complete signal channels are included. This results in cophased voltage or current output signals and eliminates the need for output demultiplexing circuitry. The monolithic AD1865 chip includes CMOS logic elements, bipolar and MOS linear elements and laser-trimmed thin-film resistor elements, all fabricated on Analog Devices' ABCMOS process.

The DACs on the AD1865 chip employ a partially segmented architecture. The first four MSBs of each DAC are segmented into 15 elements. The 14 LSBs are produced using standard R-2R techniques. Segment and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. This architecture minimizes errors at major code transitions resulting in low output glitch and eliminating the need for an external deglitcher. When used in the current output mode, the AD1865 provides two ±1 mA output signals.

Each channel is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±3 V signals at load currents up to 8 mA. Each output amplifier is short-circuit protected and can withstand indefinite short circuits to ground.

The AD1865 was designed to balance two sets of opposing requirements, channel separation and DAC matching. High channel separation is the result of careful layout. At the same time, both channels of the AD1865 have been designed to ensure matched gain and linearity as well as tracking over time and temperature. This assures optimum performance when used in stereo and multi-DAC per channel applications.

A versatile digital interface allows the AD1865 to be directly connected to standard digital filter chips. This interface employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial input pins for the left and right DAC input registers. Input data bits are clocked into the input register on the rising edge of CLK. A low-going latch edge updates the respective DAC output. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together.

The AD1865 operates with ±5 V power supplies. The digital supply, V_L, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. The AD1865 typically dissipates only 225 mW, with a maximum power dissipation of 260 mW.

The AD1865 is packaged in both a 24-pin plastic DIP and a 28-pin SOIC package. Operation is guaranteed over the temperature range of –25°C to +70°C and over the voltage supply range of ±4.75 V to ±5.25 V.

PRODUCT HIGHLIGHTS

1. The AD1865 is a complete dual 18-bit audio DAC.
2. 110 dB signal-to-noise ratio for low noise operation.
3. THD+N is typically 0.003%.
4. Interchannel gain and midscale matching.
5. Output voltages and currents are cophased.
6. Low glitch for improved sound quality.
7. Both channels are 100% tested at 16 × F_S.
8. Low Power—only 225 mW typ, 260 mW max.
9. Five-wire interface for individual DAC control.
10. 24-pin DIP or 28-pin SOIC packages available.

REV. 0

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AD1865–SPECIFICATIONS (T_A = +25°C, $+V_L$ = $+V_S$ = +5 V and $-V_S$ = –5 V, F_S = 705.6 kHz, no MSB adjustment or deglitcher)

Parameter	Min	Typ	Max	Unit
RESOLUTION		18		Bits
DIGITAL INPUTS V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, V_{IH} = $+V_L$			**1.0**	µA
I_{IL}, V_{IL} = 0.4 V			**–10**	µA
Clock Input Frequency	**13.5**			MHz
ACCURACY				
Gain Error		0.2	**1.0**	% of FSR
Interchannel Gain Matching		0.3	**0.8**	% of FSR
Midscale Error		4		mV
Interchannel Midscale Matching		5		mV
Gain Linearity (0 dB to –90 dB)		<2		dB
DRIFT (0°C to +70°C)				
Gain Drift		±25		ppm of FSR/°C
Midscale Drift		±4		ppm of FSR/°C
TOTAL HARMONIC DISTORTION + NOISE*				
0 dB, 990.5 Hz AD1865N, R		0.004	**0.006**	%
AD1865N-J, R-J		0.003	**0.004**	%
20 dB, 990.5 Hz AD1865N, R		0.010	**0.040**	%
AD1865N-J, R-J		0.010	**0.020**	%
–60 dB, 990.5 Hz AD1865N, R		1.0	**4.0**	%
AD1865N-J, R-J		1.0	**2.0**	%
CHANNEL SEPARATION*				
0 dB, 990.5 Hz	**110**	116		dB
SIGNAL-TO-NOISE RATIO* (20 Hz to 30 kHz)	**107**	110		dB
D-RANGE* (With A-Weight Filter)				
–60 dB, 990.5 Hz AD1865N, R	**88**	100		dB
AD1865N-J, R-J	**94**	100		dB
OUTPUT				
Voltage Output Configuration				
Output Range (±1%)	**±2.94**	±3.0	**±3.06**	V
Output Impedance		0.1		Ω
Load Current	±8			mA
Short Circuit Duration	Indefinite to Common			
Current Output Configuration				
Bipolar Output Range (±30%)		±1		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
$+V_L$ and $+V_S$	4.75	**5.0**	5.25	V
$-V_S$	–5.25	**–5.0**	–4.75	V
+I, $+V_L$ and $+V_S$ = +5 V		22	**26**	mA
–I, $-V_S$ = –5 V		–23	**–26**	mA
POWER DISSIPATION, $+V_L$ = $+V_S$ = +5 V, $-V_S$ = –5 V		225	**260**	mW
TEMPERATURE RANGE				
Specification	0	**+25**	+70	°C
Operation	–25		+70	°C
Storage	–60		+100	°C
WARMUP TIME	1			min

Specifications shown in **boldface** are tested on production units at final test without optional MSB adjustment.
*Tested in accordance with EIAJ Test Standard CP-307 with 18-bit data.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 V to 6.0 V
V_S to AGND . . . . . 0 V to 6.0 V
$-V_S$ to AGND . . . . . –6.0 V to 0 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . –0.3 to V_L
Short Circuit Protection . . . . . Indefinite Short to Ground
Soldering (10 sec) . . . . . +300°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1865 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	THD+N @ FS	Package Option*
AD1865N	–25°C to +70°C	0.006%	N-24A
AD1865N-J	–25°C to +70°C	0.004%	N-24A
AD1865R	–25°C to +70°C	0.006%	R-28
AD1865R-J	–25°C to +70°C	0.004%	R-28

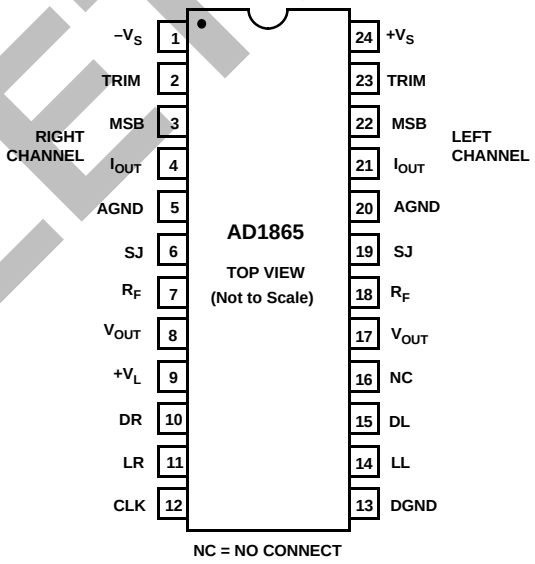
*N = Plastic DIP, R = Small Outline IC Package.

PIN DESIGNATIONS

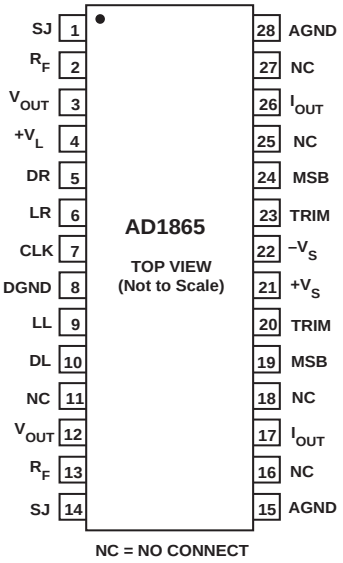
DIP	SOIC		
1	22	$-V_S$	Negative Analog Supply
2	23	TRIM	Right Channel Trim Network Connection
3	24	MSB	Right Channel Trim Potentiometer Wiper Connection
4	26	I_{OUT}	Right Channel Output Current
5	28	AGND	Analog Common Pin
6	1	SJ	Right Channel Amplifier Summing Junction
7	2	R_F	Right Channel Feedback Resistor
8	3	V_{OUT}	Right Channel Output Voltage
9	4	$+V_L$	Positive Digital Supply
10	5	DR	Right Channel Data Input Pin
11	6	LR	Right Channel Latch Pin
12	7	CLK	Clock Input Pin
13	8	DGND	Digital Common Pin
14	9	LL	Left Channel Latch Pin
15	10	DL	Left Channel Data Input Pin
16	11, 16, 18 25, 27	NC	No Internal Connection*
17	12	V_{OUT}	Left Channel Output Voltage
18	13	R_F	Left Channel Feedback Resistor
19	14	SJ	Left Channel Amplifier Summing Junction
20	15	AGND	Analog Common Pin
21	17	I_{OUT}	Left Channel Output Current
22	19	MSB	Left Channel Trim Potentiometer Wiper Connection
23	20	TRIM	Left Channel Trim Network Connection
24	21	$+V_S$	Positive Analog Supply

*Pin 16 has no internal connection; $-V_L$ from AD1864 DIP socket can be safely applied.

PINOUT
(24-Pin DIP Package)



(28-Pin SOIC Package)



TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent.

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large (0 dB) and small (–20 dB, –60 dB) signal amplitudes. THD+N measurements for the AD1865 are made using the first 19 harmonics and noise out to 30 kHz.

SIGNAL-TO-NOISE RATIO

The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale code is entered to the amplitude of the output when a midscale code is entered. It is measured using a standard A-Weight filter. SNR for the AD1865 is measured for noise components out to 30 kHz.

CHANNEL SEPARATION

Channel separation is defined as the ratio of the amplitude of a full-scale signal appearing on one channel to the amplitude of that same signal which couples onto the adjacent channel. It is usually expressed in dB. For the AD1865 channel separation is measured in accordance with EIAJ Standard CP-307, Section 5.5.

D-RANGE DISTORTION

D-Range distortion is equal to the value of the total harmonic distortion + noise (THD+N) plus 60 dB when a signal level of –60 dB below full scale is reproduced. D-Range is tested with a 1 kHz input sine wave. This is measured with a standard A-Weight filter as specified by EIAJ Standard CP-307.

GAIN ERROR

The gain error specification indicates how closely the output of a given channel matches the ideal output for given input data. It is expressed in % of FSR and is measured with a full-scale output signal.

INTERCHANNEL GAIN MATCHING

The gain matching specification indicates how closely the amplitudes of the output signals match when producing identical input data. It is expressed in % of FSR (Full-Scale Range = 6 V for the AD1865) and is measured with full-scale output signals.

MIDSCALE ERROR

Midscale error is the deviation of the actual analog output of a given channel from the ideal output (0 V) when the twos complement input code representing half scale is loaded into the input register of the DAC. It is expressed in mV and is measured with half-scale output signals.

INTERCHANNEL MIDSCALE MATCHING

The midscale matching specification indicates how closely the amplitudes of the output signals of the two channels match when the twos complement input code representing half scale is loaded into the input register of both channels. It is expressed in mV and is measured with half-scale output signals.

FUNCTIONAL DESCRIPTION

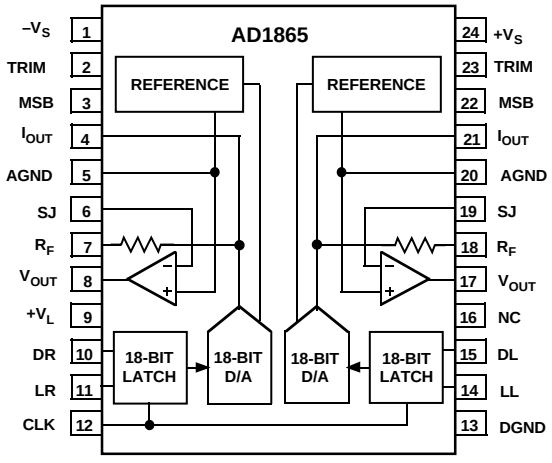
The AD1865 is a complete, monolithic, dual 18-bit audio DAC. No external components are required for operation. As shown in the block diagram, each chip contains two voltage references, two output amplifiers, two 18-bit serial input registers and two 18-bit DACs.

The voltage reference section provides a reference voltage for each DAC circuit. These voltages are produced by low-noise bandgap circuits. Buffer amplifiers are also included. This combination of elements produces reference voltages that are unaffected by changes in temperature and age.

The output amplifiers use both MOS and bipolar devices and incorporate an all NPN output stage. This design technique produces higher slew rate and lower distortion than previous techniques. Frequency response is also improved. When combined with the appropriate on-chip feedback resistor, the output op amps convert the output current to output voltages.

The 18-bit D/A converters use a combination of segmented decoder and R-2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser trimming of these resistors further reduces linearity errors resulting in low output distortion.

The input registers are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption, contributing to the low glitch and low power dissipation of the AD1865.



AD1865 Block Diagram (DIP Package)

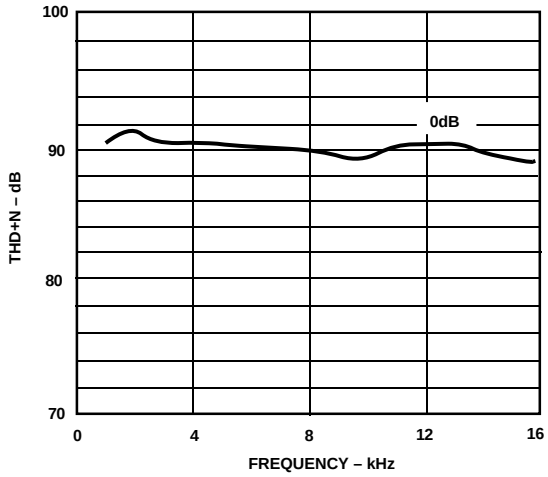


Figure 1. THD+N (dB) vs. Frequency (kHz)

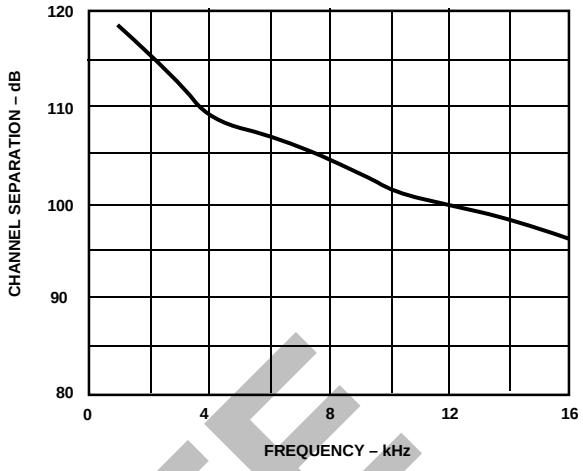


Figure 2. Channel Separation (dB) vs. Frequency (kHz)

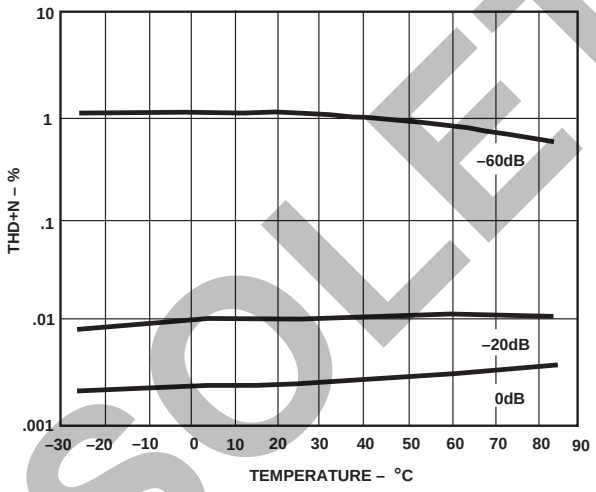


Figure 3. THD+N (%) vs. Temperature (°C)

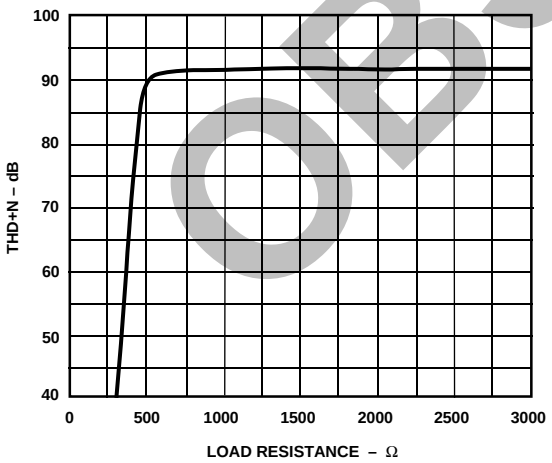


Figure 4. THD+N (dB) vs. Load Resistance (Ω)

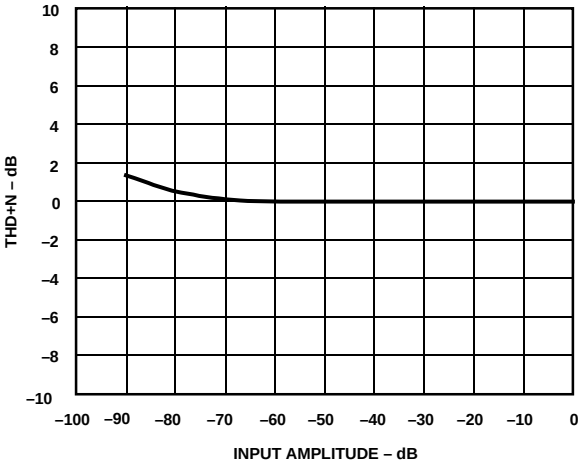


Figure 5. Gain Linearity (dB) vs. Input Amplitude (dB)

AD1865–Analog Circuit Consideration

GROUNDING RECOMMENDATIONS

The AD1865 has three ground pins, two labeled AGND and one labeled DGND. AGND, the analog ground pins, are the "high quality" ground references for the device. To minimize distortion and reduce crosstalk between channels, the analog ground pins should be connected together only at the analog common point in the system. As shown in Figure 6, the AGND pins should not be connected at the chip.

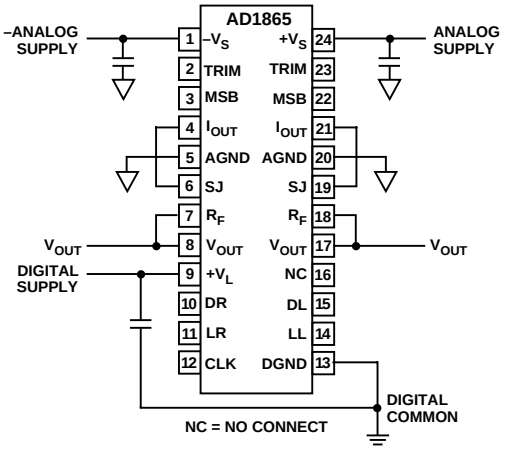


Figure 6. Recommended Circuit Schematic

The digital ground pin returns ground current from the digital logic portions of the AD1865 circuitry. This pin should be connected to the digital common pin in the system. Other digital logic chips should also be referred to that point. The analog and digital grounds should be connected together at one point in the system, preferably at the power supply.

POWER SUPPLIES AND DECOUPLING

The AD1865 has three power supply input pins. $\pm V_S$ provides the supply voltages which operate the analog portions of the DAC including the voltage references, output amplifiers and control amplifiers. The $\pm V_S$ supplies are designed to operate from ±5 V supplies. Each supply should be decoupled to analog common using a 0.1 µF capacitor in parallel with a 10 µF capacitor. Good engineering practice suggests that the bypass capacitors be placed as close as possible to the package pins. This minimizes the parasitic inductive effects of printed circuit board traces.

The $+V_L$ supply operates the digital portions of the chip including the input shift registers and the input latching circuitry. This supply should be bypassed to digital common using a 0.1 µF capacitor in parallel with a 10 µF capacitor. $+V_L$ operates with a +5 V supply. In order to assure proper operation of the AD1865, $-V_S$ must be the most negative power supply voltage at all times.

Though separate positive power supply pins are provided for the analog and digital portions of the AD1865, it is also possible to use the AD1865 in systems featuring a single +5 V power supply. In this case, both the $+V_S$ and $+V_L$ input pins should be connected to the single +5 V power supply. This feature allows reduction of the cost and complexity of the system power supply.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of an audio system.

DISTORTION PERFORMANCE AND TESTING

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD+N specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance. Figure 1 illustrates the typical THD+N performance of the AD1865 versus frequency. A load impedance of at least 1.5 kΩ is recommended for best THD+N performance.

Analog Devices tests and grades all AD1865s on the basis of THD+N performance. During the distortion test, a high-speed digital pattern generator transmits digital data to each channel of the device under test. Eighteen-bit data is transmitted at 705.6 kHz ($16 \times F_S$). The test waveform is a 990.5 Hz sine wave with 0 dB, –20 dB and –60 dB amplitudes. A 4096 point FFT calculates total harmonic distortion + noise, signal-to-noise ratio, D-Range and channel separation. No deglitchers or MSB trims are used in the testing of the AD1865.

OPTIONAL MSB ADJUSTMENT

Use of optional adjust circuitry allows residual distortion error to be eliminated. This distortion is especially important when low amplitude signals are being reproduced. The MSB adjust circuitry is shown in Figure 7. The trim potentiometer should be adjusted to produce the lowest distortion using an input signal with a –60 dB amplitude.

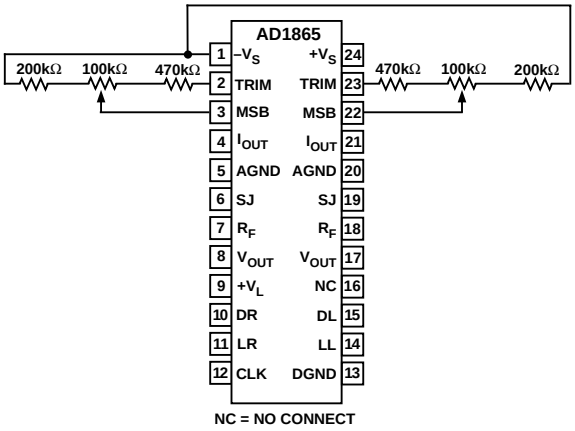


Figure 7. Optional THD+N Adjust Circuitry

CURRENT OUTPUT MODE

One or both channels of the AD1865 can be operated in current output mode. I_{OUT} can be used to directly drive an external current-to-voltage (I-V) converter. The internal feedback resistor, R_F, can still be used in the feedback path of the external I-V converter, thus assuring that R_F tracks the DAC over time and temperature.

Of course, the AD1865 can also be used in voltage output mode in order to utilize the onboard I-V converter.

VOLTAGE OUTPUT MODES

As shown on the block diagram, each channel of the AD1865 is complete with an I-V converter and a feedback resistor. These can be connected externally to provide direct voltage output from one or both AD1865 channels. Figure 6 shows these connections. I_{OUT} is connected to the Summing Junction, SJ. V_{OUT} is connected to the feedback resistor, R_F. This implementation results in the lowest possible component count and achieves the specifications shown on the Specifications page while operating at $16 \times F_S$.

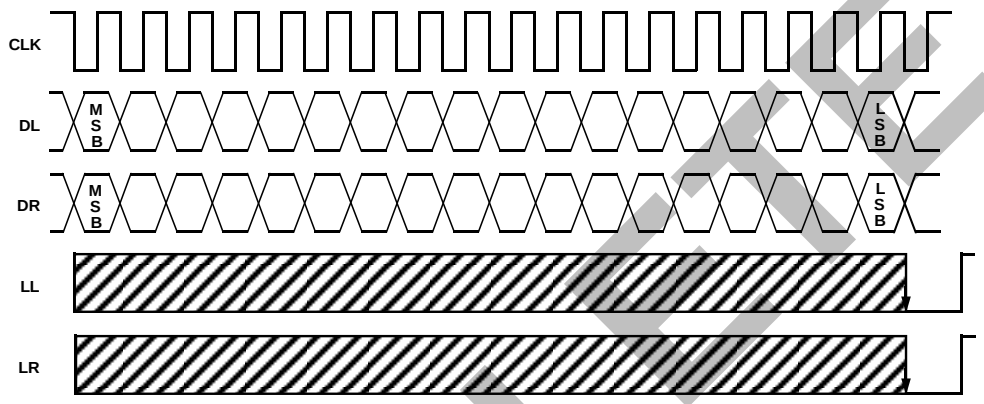


Figure 8. AD1865 Control Signals

INPUT DATA

Data is transmitted to the AD1865 in a bit stream composed of 18-bit words with a serial, twos complement, MSB first format. Data Left (DL) and Data Right (DR) are the serial inputs for the left and right DACs, respectively. Similarly, Latch Left (LL) and Latch Right (LR) update the left and right DACs. The falling edge of LL and LR cause the last 18 bits which were clocked into the Serial Registers to be shifted into the DACs, thereby updating the DAC outputs. Left and Right channels share the Clock (CLK) signal. Data is clocked into the input registers on the rising edge of CLK.

Figure 8 illustrates the general signal requirements for data transfer for the AD1865.

TIMING

Figure 9 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1865 are both TTL and 5 V CMOS compatible.

The minimum clock rate of the AD1865 is at least 13.5 MHz. This clock rate allows data transfer rates of 2×, 4×, 8× and $16 \times F_S$ (where F_S equals 44.1 kHz).

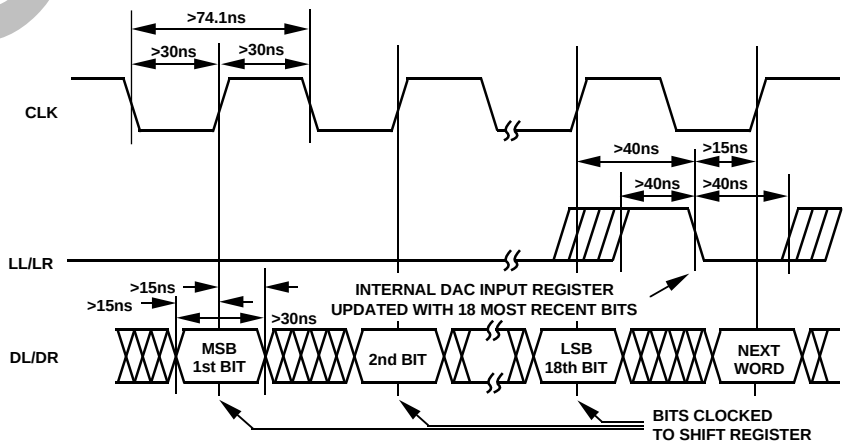


Figure 9. AD1865 Timing Diagram

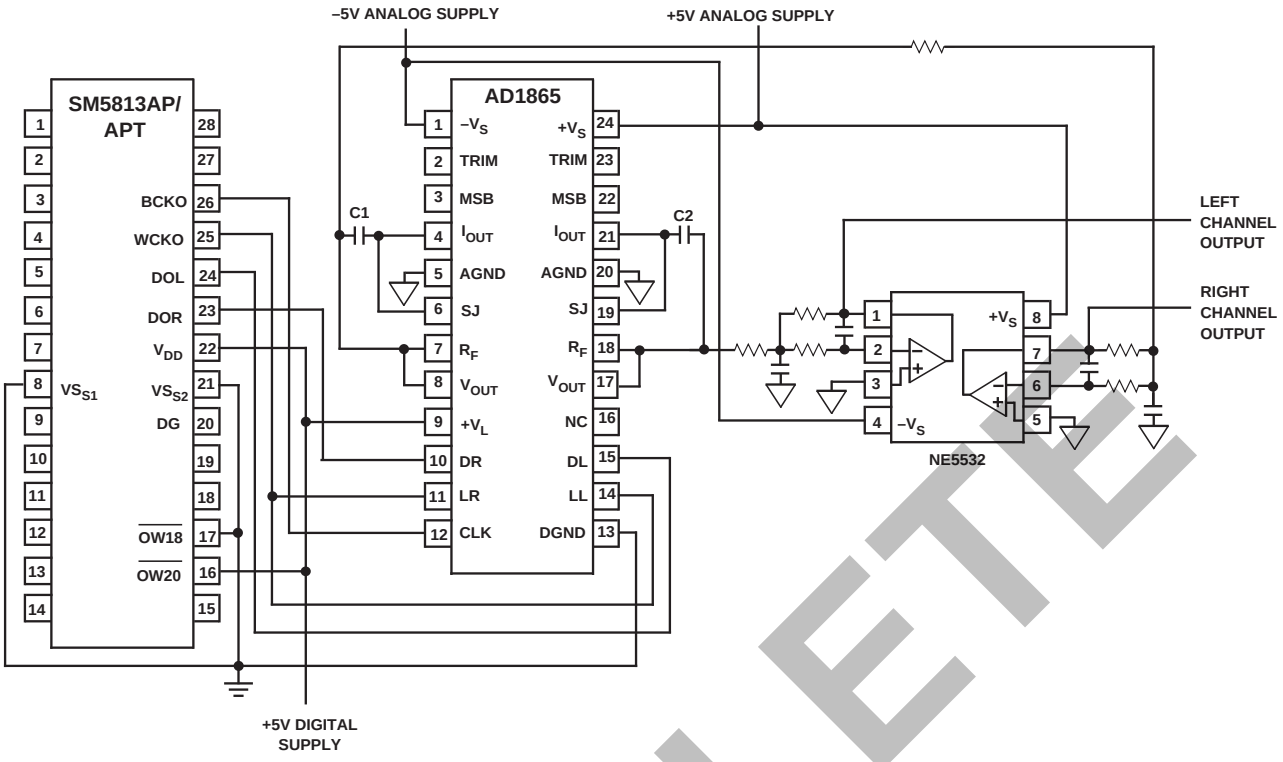


Figure 10. Complete 8 × F_S 18-Bit CD Player

18-BIT CD PLAYER DESIGN

Figure 10 illustrates an 18-bit CD player design incorporating an AD1865 D/A converter, an NE5532 dual op amp and the SM5813 digital filter chip manufactured by NPC. In this design, the SM5813 filter transmits left and right digital data to both channels of the AD1865. The left and right latch signals, LL and LR, are both provided by the word clock signal (WCKO) of the digital filter. The digital filter supplies data at an 8 × F_S oversample rate to each channel.

The digital data is converted to analog output voltages by the output amplifiers on the AD1865. Note that no external components are required by the AD1865. Also, no deglitching circuitry is required.

An NE5532 dual op amp is used to provide the output antialias filters required for adequate image rejection. One 2-pole filter section is provided for each channel. An additional pole is created from the combination of the internal feedback resistors (R_F) and the external capacitors C1 and C2. For example, the nominal 3 kΩ R_F with a 360 pF capacitor for C1 and C2 will place a pole at approximately 147 kHz, effectively eliminating all high frequency noise components.

Low distortion, superior channel separation, low power consumption and a low parts count are all realized by this simple design.

MULTICHANNEL DIGITAL KEYBOARD DESIGN

Figure 11 illustrates how to cascade AD1865's to add multiple voices to an electronic musical instrument. In this example, the data and clock signals are shared between all six DACs. As the data representing an output for a specific voice is loaded, the appropriate DAC is updated. For example, after the 18-bits representing the next output value for Voice 4 is clocked out on the data line, then "Voice 4 Load" is pulled low. This produces a new output for Voice 4. Furthermore, all voices can be returned to the same output by pulling all six load signals low.

In this application, the advantages of choosing the AD1865 are clear. Its flexible digital interface allows the clock and data to be shared among all DACs. This reduces PC board area requirements and also simplifies the actual layout of the board. The low power requirements of the AD1865 (approximately 225 mW) is an advantage in a multiple DAC system where any power advantage is multiplied by the number of DACs used. The AD1865 requires no external components, simplifying the design, reducing the total number of components required and enhancing reliability.

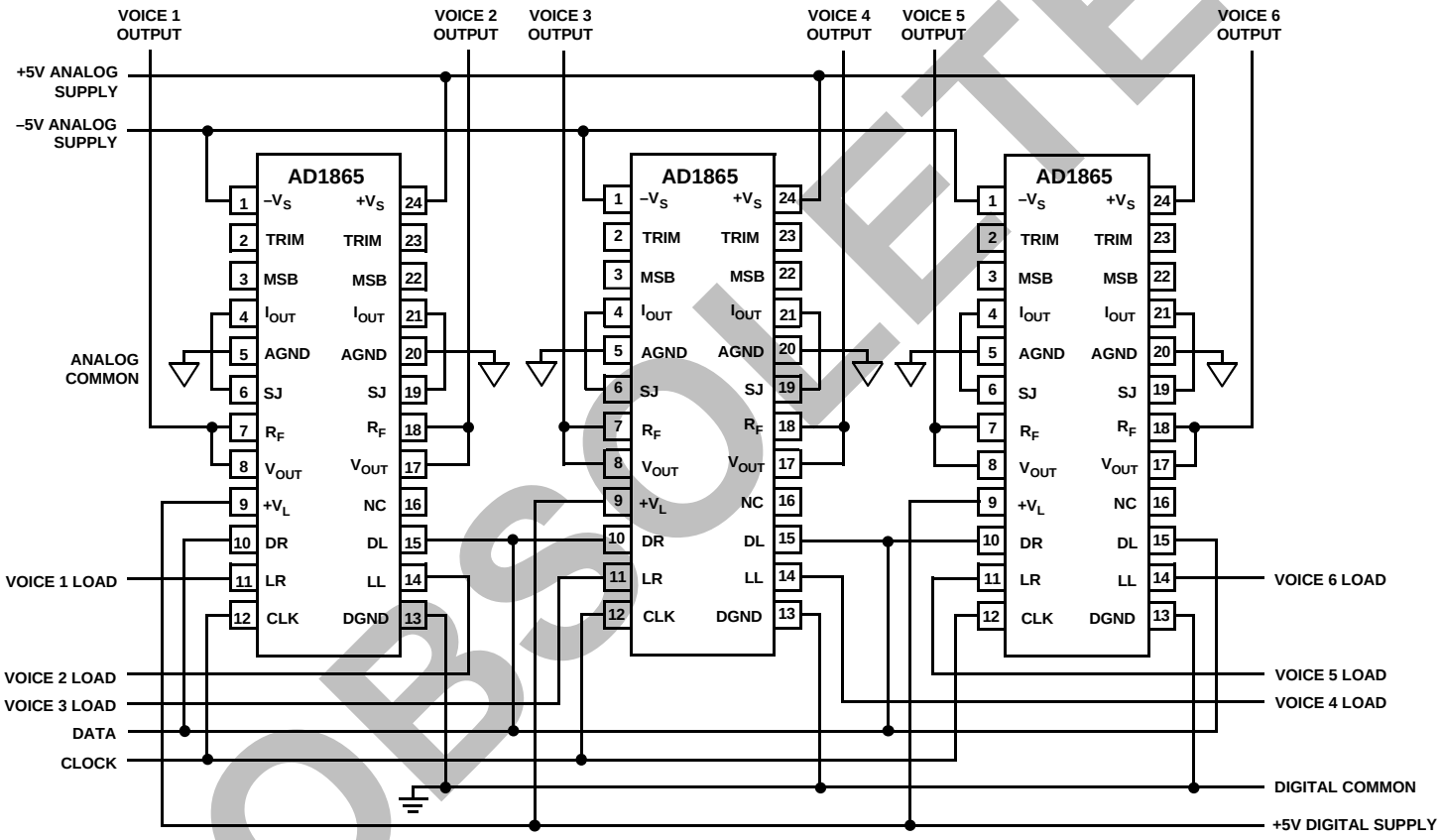


Figure 11. Cascaded AD1865s in a Multichannel Keyboard Instrument

ADDITIONAL APPLICATIONS

Figures 12 through 14 show connection diagrams for the AD1865 and standard digital filter chips from Yamaha, NPC and Sony. Each figure is an example of cophase operation operating at $8 \times F_S$ for each channel. The 2-pole Rauch low-pass filters shown in Figure 10 can be used with all of the applications shown in this data sheet.

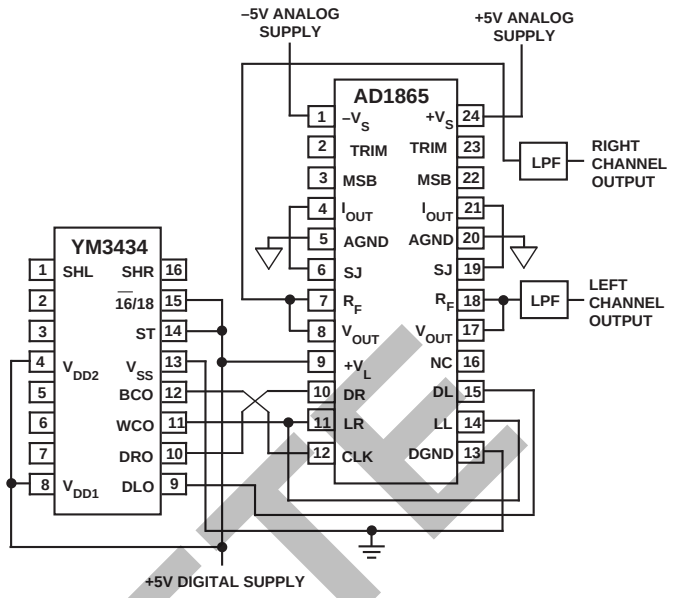


Figure 12. AD1865 with Yamaha YM3434 Digital Filter

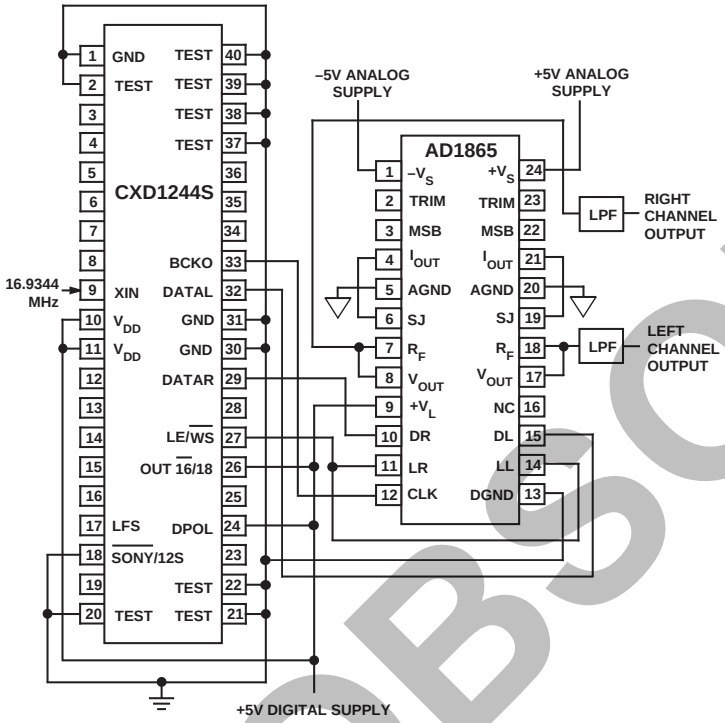


Figure 13. AD1865 with Sony CXD1244s Digital Filter

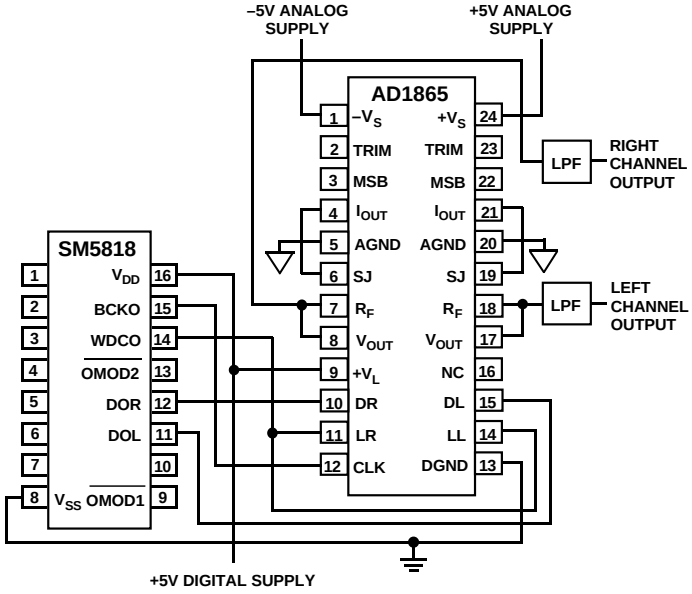
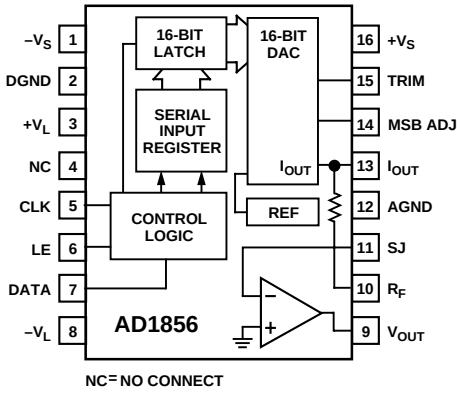
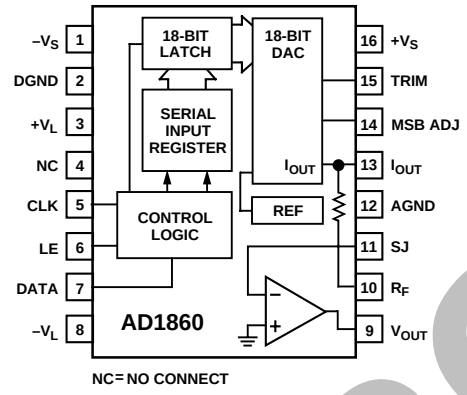


Figure 14. AD1865 with NPC SM5818AP Digital Filter

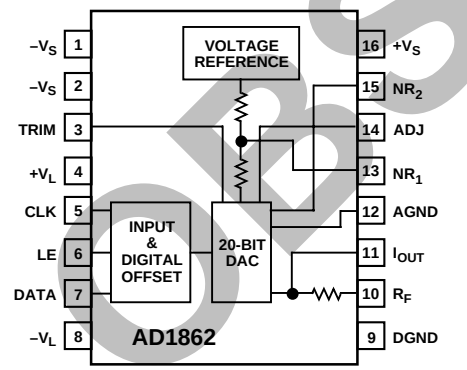
OTHER DIGITAL AUDIO COMPONENTS AVAILABLE FROM ANALOG DEVICES



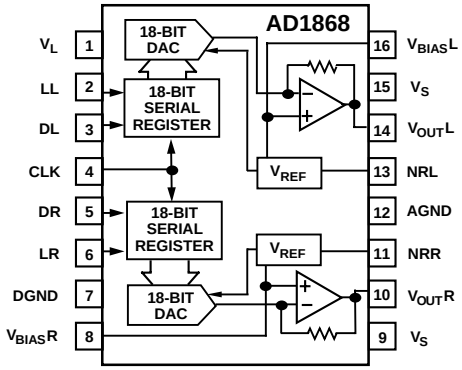
AD1856 16-BIT AUDIO DAC
Complete, No External Components Required
0.0025% THD
Low Cost
16-Pin DIP or SOIC Package
Standard Pinout



AD1860 18-BIT AUDIO DAC
Complete, No External Components Required
0.0025% THD+N
108 dB Signal-to-Noise Ratio
16-Pin DIP or SOIC Package
Standard Pinout



AD1862 20-BIT AUDIO DAC
119 dB Signal-to-Noise Ratio
0.0016% THD+N
102 dB D-Range Performance
±1 dB Gain Linearity
16-Pin DIP Package

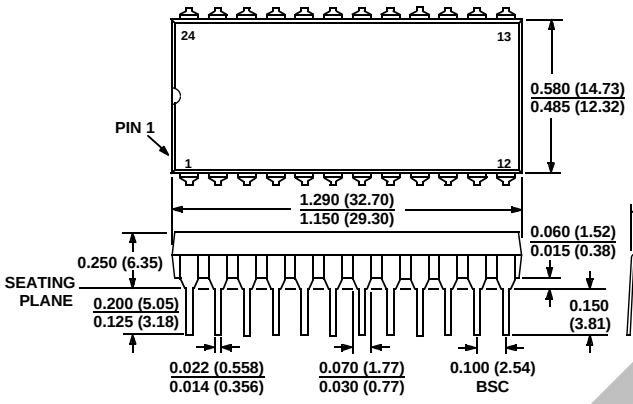


AD1868 +5 V SINGLE SUPPLY DUAL 18-BIT AUDIO DAC
No External Components Required
0.004% THD+N
92 dB D-Range Performance
±3 dB Gain Linearity
16-Pin DIP or SOIC Package

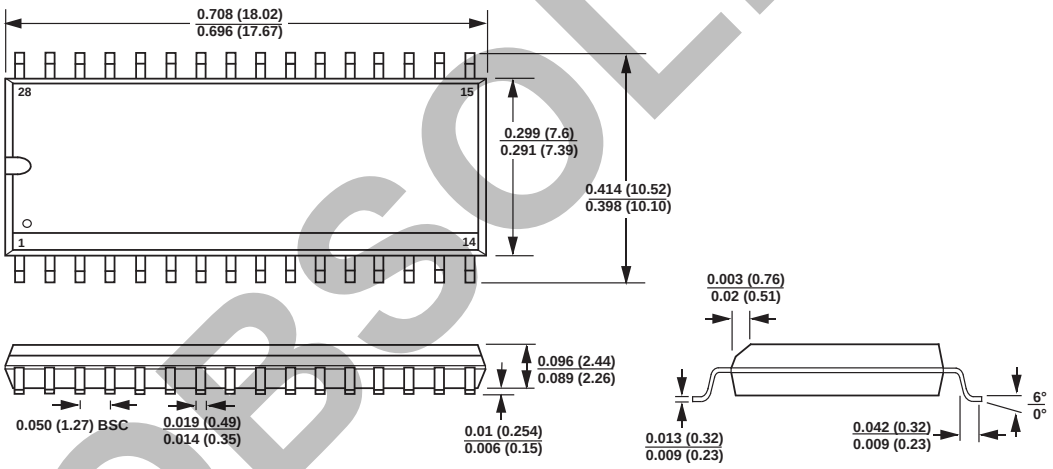
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Pin Plastic DIP
(N-24A) Package



28-Pin SOIC
(R-28) Package



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